removed or partially removed). Then, semiconductor material is epitaxially deposited in the trench.

[Para 17] The wafer is preferably planarized after the trench is filled with epitaxially deposited material. The SOI region and bulk region may be doped with different dopants, so that a P-N junction is formed in the trench or in the SOI region. A metal silicide layer may be deposited over the trench to form an electrical contact bridging the SOI region and bulk region.

[Para 18] Description of the Figures

[Para 19] Fig. 1 shows a hybrid SOI/bulk CMOS integrated circuit device according to the present invention.

[Para 20] Fig. 2a shows an embodiment of the invention in which a P-N butted junction overlaps a boundary between SOI and bulk device regions.

[Para 21] Fig. 2b shows an embodiment of the invention in which an epitaxy filled trench extends down to a buried oxide layer of the SOI region.

[Para 22] ~~Figs. 3a-3l~~ Figs. 3a-3k illustrate a preferred method for making the integrated circuit of the present invention.

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[Para 23] Fig. 4 shows an alternative embodiment of the present invention.

[Para 24] Fig. 5 shows an alternative embodiment of the present invention in which p+ and n+ doped regions do not extend deeply.

[Para 25] Detailed Description of the preferred embodiments

[Para 26] The present invention provides an integrated circuit having devices fabricated in both SOI regions and bulk regions. The SOI and bulk